Bibrak Qamar Chandio

AI Computing Systems Laboratory (AICSL)
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CAREER SUMMARY

Application and runtime software developer for scalable high performance computing who has worked on both ends of scalable software development from design and implementation of runtime systems (like MPI) to implementation of scientific and data applications on clusters, shared memory, GPU and PGAS platforms.

EDUCATION

Indiana University, Bloomington, IN, USA — May-2022 (expected)
Doctor of Philosophy in Intelligent Systems Engineering
Minor: Scientific Computing

Indiana University, Bloomington, IN, USA — May-2016
Master of Science in Computer Science
Under Fulbright Scholarship

National University of Sciences and Technology, Islamabad, Pakistan — May-2011
Bachelor of Science in Information Technology
Under Prime Minister's National ICT Scholarship

Main Technical AREAS

HPC, Parallel Computing, MPI, Java MPI, Scientific Computing, Graph Processing, GPU Computing

WORK EXPERIENCE

Intel
Hillsboro, Oregon USA — May 2021 – Nov 2021 (as planed)
Technical Consulting Engineer - Graduate Intern

- Designing test code for benchmarking One MKL math library features against competition. Benchmarking the code and designing run scripts that enable easy comparison in the future by any Intel Technical Consultant.
- Second part of the internship involves scaling GPU FFT on the new Intel multi-tile architecture. From a single tile to multiple tiles on a single GPU to multi-GPUs on a node and then later to a cluster setting. This work is in progress.

AI Computing Systems Laboratory (AICSL) (previously CREST)
Indiana University, Bloomington USA — Aug 2018 – Present
Graduate Student and Associate Instructor

- Exploring the design space for graph primitives for non-von Neumann architectures like the Continuum Computer Architecture (CCA), where small homogenous computing cores with their own memory are arranged in a PIM fashion to enable low-latency and highly parallel asynchronous message driven computing.
- I teach, grade and manage the High Performance Computing course for graduate and undergraduate students at Indiana University with my advisor Prof. Thomas Sterling.
- Mentoring and managing undergraduate students to conduct research and development. Each semester, I take on one or two students and introduce them to basics of HPC and Parallel Computing and then work with them to find an interesting problem area that could use HPC. Students end up learning not just coding in parallel but also deploying solutions on supercomputers to presenting their work in front of

their peers in the form of posters. I believe parallel programming needs to be basic part of undergraduate education.

Advanced Micro Devices (AMD) Research
Austin, Texas USA May 2020 – Aug 2020
Co-Op Engineer

- Designed, and profiled Sparse Triangular Solvers that used only a single kernel across distributed multi-GPU system.
- This helped achieve low latency by directly communicating from within the kernel to other GPUs using PGAS.
- It also reduced the amount of overhead that would have incurred due to multiple kernel launches.
- In short, using such dynamic fine-grain computation we not only achieved improvements in performance but also exposed parallelism that would have been sacrificed due to no dynamic communication ability offered by conventional programming models.

Advanced Micro Devices (AMD) Research
Austin, Texas USA Jun 2018 – Aug 2018
Co-Op Engineer

- Designed, developed, and profiled candidate applications and kernels for a new low latency distributed multi GPU intra-kernel communication runtime system (and programming model).

Center for Research in Extreme Scale Technologies
Indiana University, Bloomington USA Aug 2016 – May 2018
Graduate Student and Research Associate

- Application development on top of dynamic adaptive runtime systems for Exascale computing, in particular HPX).
- Example: Molecular Dynamics application on top of HPX
  - https://github.com/bibrakc/hpx/tree/main/hpx-apps/CoMD
- Performance evaluation and tuning for applications on top of HPX.
- Researching Graph processing under an asynchronous event driven (active message like) execution regime.

HPC Lab, National University of Sciences and Technology, Islamabad, Pakistan Aug 2013 – June 2014
Developer

- Developer of an open source Java message-passing library called MPJ Express http://mpjexpress.org that allows application developers to write and execute parallel applications for multicore processors and compute clusters/clouds.
- Contributed in design, development, testing and performance tuning of new communication devices for MPJ Express. In particular, developed a native device to enable MPJ Express to use native MPI libraries for communication and a hybrid device to exploit hybrid parallelism transparently.
- Published a paper in ICCS 2014.
- Published a paper in the Journal of Parallel Computing 2015.

HPC Lab UAE University, Al Ain, UAE Oct 2011 - May 2013
Assistant Researcher

- Oil Reservoir Simulation on GPUs and MPI based clusters.
- Design and evaluated scheduling algorithms for divisible load applications in heterogeneous cloud environments.

TECHNICAL SKILLS

Programming Languages/models: C/C++, CUDA, Maxeler DataFlow, Java, MPI, OpenMP, R

Scripting Languages: bash script
Development Tools & Editors: vi, netbeans, eclipse
Operating Systems: Linux, OS X, Windows

JOURNAL PAPERS

Ansar Javed, **Bibrak Qamar**, Mohsan Jameel, Aamir Shafi, Bryan Carpenter **Towards Scalable Java HPC with Hybrid and Native Communication Devices in MPJ Express**, International Journal of Parallel Programming, 2015, pp 1-31

CONFERENCE PAPERS

Bibrak Qamar, Ansar Javed, Mohsan Jameel, Aamir Shafi and Bryan Carpenter **Design and Implementation of Hybrid and Native Communication Devices for Java HPC**, Procedia Computer Science 29 (2014) 184–197

WORKSHOP PAPERS

Fadi N. Sibai, Saadullah Mohammad, Hashir Karim Kidwai, **Bibrak Qamar**, Falah Awwad: **Parallel Implementation and Performance Analysis of a 3D Oil Reservoir Data Visualization Tool on the Cell Broadband Engine and CUDA GPU**, HPCC-ICESS 2012: 970-975

POSTERS

Bibrak Qamar, Prateek Srivastava: **Asynchronous Graph Processing Using Message Driven Systems,** 2019 R-CCS International Symposium

SOME ACADEMIC PROJECTS

- Implemented a **parallel construct** called *let-par* for a basic scheme like functional programming language. *let-par* makes parallel programing easy by removing the dirty work of exposing, managing and tuning parallelism from the programmer. *let-par* executes let bindings in parallel using POSIX threads, which aims to make the language portable across system software and hardware. *let-par* is implemented in such a way that it also exploits nested parallelism from with in *let-pars*, think of a recursive function that calls *let-par*.
  - Poster: https://homes.soic.indiana.edu/bchandio/source/Poster_LPL.pdf
- Ported Molecular Dynamics application on to dynamic adaptive runtime system (HPX) during my masters in Computer Science. https://github.com/bibrakc/hpx/tree/main/hpx-apps/CoMD
- My Undergraduate Final Year Project was **Implementation and Evaluation of Scientific Simulations on HPC Architectures**. My main job was to parallelize **Conjugate Gradient** Method (an iterative method for solving System of Linear Equations) on Distributed Memory machines, Shared Memory machines and Accelerators (GPUs) and analyze the performance, cost and efficiency.
  - Report/Documentation: http://bit.ly/2d9LCAN
  - Poster: http://bit.ly/2dF0D2u
  - Demo Simulation: http://www.youtube.com/watch?v=J6J0TO0Q_MQ

HONORS & AWARDS

- Student travel award for the 2019 7th Annual **MVAPICH User Group (MUG)** Meeting and presented poster: https://github.com/bibrakc/HPX_graphs/blob/main/Reports_and_Posters/Poster%20MUG.pdf
- Student travel award for the 2019 1st **R-CCS International Symposium** and **R-CCS Youth Workshop Japan**.

- Recipient of the **Fulbright** Masters Scholarship 2014 (MS Computer Science from Indiana University Bloomington, IN, United States)
- Recipient of the merit based **Prime Minister's National ICT Scholarship** for undergraduate studies at NUST for 4 years of BS in IT.
- Participated as student in **2nd International Summer School on High Performance, Grid/Cloud Computing** held in UAE University Al Ain **UAE**.
- Participated in **Microsoft Imagine Cup** 2010. Our idea qualified to semifinal. The theme was to use technology to help solve world's toughest problems. The idea was "**Secure Donation**", a system that can track where the donation is being spent. This will ultimately encourage donors and make charities more transparent.

MENTORING

Spring 2019	**Harrison Yelton** (Undergrad)
Poster Title:	Uncovering Network Properties: What Can we Learn?
Area:	Parallel graph processing

Fall 2019	**Gourav Pullela** (Undergrad) and **Riley Campbell** (Undergrad)
Poster Title:	RSA Encryption using High Performance Computing
Area:	Parallel encryption and decryption

Fall 2020	**Nrushad Joshi** (Undergrad)
Poster Title:	Matrix Vector Multiplication on Bigred3 Supercomputer
Area:	Parallel matrix vector multiplication